REMARKS

Claims 22-36 are pending in the application.

Claims 22-24, 26-28, 30-32 and 34-35 are rejected as being anticipated by SHIBATA 5,442,755. This rejection is respectfully traversed.

Claim 22 recites a plurality of processors which send and receive predetermined information to and from each other. Claim 22 further recites that once each of the plurality of processors has accessed the shared memory, when one of the plurality of processors updates a predetermined data in the shared memory, the one of the plurality of processors requests others of the plurality of processors to access the updated predetermined data from the shared memory.

SHIBATA discloses a multiprocessor system having a shared memory. The multiprocessor system of SHIBATA uses a shared memory for data storage and does not disclose or suggest that a plurality of processors send and receive information to and from each other.

Moreover, in the contention scenario of SHIBATA, a first processor accesses the shared memory and then a second processor accesses the shared memory. After the second (or final processor) accesses the shared memory, the sequence of accessing the shared memory is complete. SHIBATA does not teach or suggest that once each of the plurality of processors has accessed the shared memory, when one of the plurality of processors updates a

predetermined data in the shared memory, that one of the plurality of processors requests others of the plurality of processors to access the updated predetermined data from the shared memory. Specifically, SHIBATA teaches neither updating predetermined data nor one processor requesting other processors to access updated predetermined data.

As the reference does not disclose that which is recited, the anticipation rejection as to claim 22 is not viable. Claims 23 and 24 depend from claim 22 and further define the invention and are also believed patentable over SHIBATA.

Independent claim 26 recites a plurality of processors which send and receive a predetermined signal to and from each other. Claim 26 also recites that once each of the plurality of processors has accessed the shared memory, when one of the plurality of processors updates a predetermined data in the shared memory, then that one of the plurality of processors outputs a re-read request signal to another of the plurality of processors, so as to request the others of the plurality of processors to access the updated predetermined data from the shared memory.

As set forth above, SHIBATA neither teaches that the plurality of processors sends and receives a predetermined signal to and from each other nor that one of the plurality of processors updates the predetermined data. The analysis above regarding claim 22 is equally applicable to claim 26 as to these

features. In addition, SHIBATA fails to disclose or suggest that one of the plurality of processors outputs a re-read request signal to another of the plurality of processors as recited.

As the reference does not disclose that which is recited, the anticipation rejection is not viable. Reconsideration and withdrawal of the rejection as to claim 26 are respectfully requested. Claims 27 and 28 depend from claim 26 and further define the invention and are also believed patentable over SHIBATA.

Claim 30 recites requesting others of a plurality of processors to perform a second access to a shared memory, when a first access to the shared memory has been done.

As set forth above, SHIBATA teaches that a plurality of processors perform a sequential single access to a shared memory. SHIBATA does not teach or suggest the processors performing a second access to a shared memory.

As the reference does not disclose that which is recited, reconsideration and withdrawal of the rejection as to claim 30 are respectfully requested. Claims 31 and 32 depend from claim 30 and further define the invention and are also believed patentable over SHIBATA.

Independent claims 34 and 35 also recite performing first and second accesses to the shared memory. Claims 34 and 35 also recite updating a predetermined data in the shared memory and requesting others of the plurality of processors to access

the updated predetermined data from the shared memory. The analysis above regarding claims 22 and 30 as it applies to these features is equally applicable to claims 34 and 35. Accordingly, claims 34 and 35 are also believed patentable over SHIBATA.

Claims 25, 29 and 33 are rejected as unpatentable over SHIBATA in view of AZEVEDO et al. 6,496,890. This rejection is respectfully traversed.

AZEVEDO is only cited for the teaching of performing a request after a predetermined period of time to reset all devices on a shared bus. AZEVEDO does not teach or suggest what is recited in claims 22, 26 and 30. As set forth above, SHIBATA does not disclose or suggest what is recited in claims 22, 26 and 30. Since claims 25, 29 and 33 depend from claims 22, 26 and 30, respectively, and further define the invention, the proposed combination of references would not render obvious claims 25, 29 and 33.

Claim 36 is rejected as unpatentable over SHIBATA in view of MOGUL 6,704,798. This rejection is respectfully traversed.

MOGUL is only cited for the teaching of embedding a data signal in a carrier wave. MOGUL does not teach performing a first access and performing a second access to a shared memory. MOGUL also does not teach that when one processor updates a predetermined data in a shared memory, that one processor requests others of the plurality of processors to access updated

predetermined data from the shared memory. As set forth above, SHIBATA does not disclose or suggest these features.

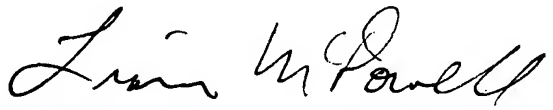
The above-noted features are missing from each of the references, are absent from the combination, and thus are not obvious to one having ordinary skill in the art.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



Liam McDowell, Reg. No. 44,231
745 South 23rd Street
Arlington, VA 22202
Telephone (703) 521-2297
Telefax (703) 685-0573
(703) 979-4709

LM/lrs